Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-10. (canceled)

11. (new) An electronic memory component, comprising:

a receiving substrate, wherein the receiving substrate is doped;

a memory cell matrix embedded in the receiving substrate;

a top/protective substrate to at least partially surround the receiving substrate on at least one side of the receiving substrate remote from the memory cell matrix, wherein the top/protective substrate is doped opposite to the receiving substrate; and

a circuit arrangement in contact with at least one substrate of the receiving substrate and the top/protective substrate for detection of a voltage or a current in response to generation of charge carriers in the at least one substrate upon light incidence on the electronic memory component.

12. (new) The electronic memory component of claim 11, wherein the circuit arrangement comprises a comparator circuit.

13. (new) The electronic memory component of claim 12, wherein the comparator circuit is connected with the receiving substrate, via an electrical contact, to detect the voltage or the current in the receiving substrate.

14. (new) The electronic memory component of claim 12, wherein the comparator circuit is connected with the top/protective substrate, via an electrical contact, to detect the voltage or the current in the top/protective substrate.

15. (new) The electronic memory component of claim 11, wherein the electronic memory component is configured to deny access to the memory component in response

to detection by the circuit arrangement of the voltage in excess of a limit voltage or the current in excess of a limit current.

16. (new) The electronic memory component of claim 11, wherein the electronic memory component is configured to emit an alarm to a controlling central processing unit (CPU) in response to detection by the circuit arrangement of the voltage in excess of a limit voltage or the current in excess of a limit current.

17. (new) The electronic memory component of claim 11, wherein the top/protective substrate comprises a well to surround the receiving substrate.

18. (new) The electronic memory component of claim 11, further comprising a carrier substrate, wherein the top/protective substrate is associated with the carrier substrate.

19. (new) The electronic memory component of claim 18, wherein the top/protective substrate is buried in the carrier substrate.

20. (new) The electronic memory component of claim 18, wherein:
the receiving substrate comprises a p-doped substrate;
the top/protective substrate comprises an n-doped substrate; and
the carrier substrate comprises another p-doped substrate.

21. (new) The electronic memory component of claim 11, further comprising:
an external source associated with the memory cell matrix, wherein the external source comprises a contact;
a bitline associated with the memory cell matrix;
a wordline associated with the memory cell matrix; and
a control gate associated with the memory cell matrix.

22. (new) The electronic memory component of claim 11, wherein the electronic memory component comprises an erasable programmable read only memory (EPROM), an electrical erasable programmable read only memory (EEPROM), or a Flash memory.

23. (new) The electronic memory component of claim 11, wherein the electronic memory component is configured to continuously detect for light incidence in the form of a light attack.

24. (new) The electronic memory component of claim 11, wherein the electronic memory component is on a smart card.